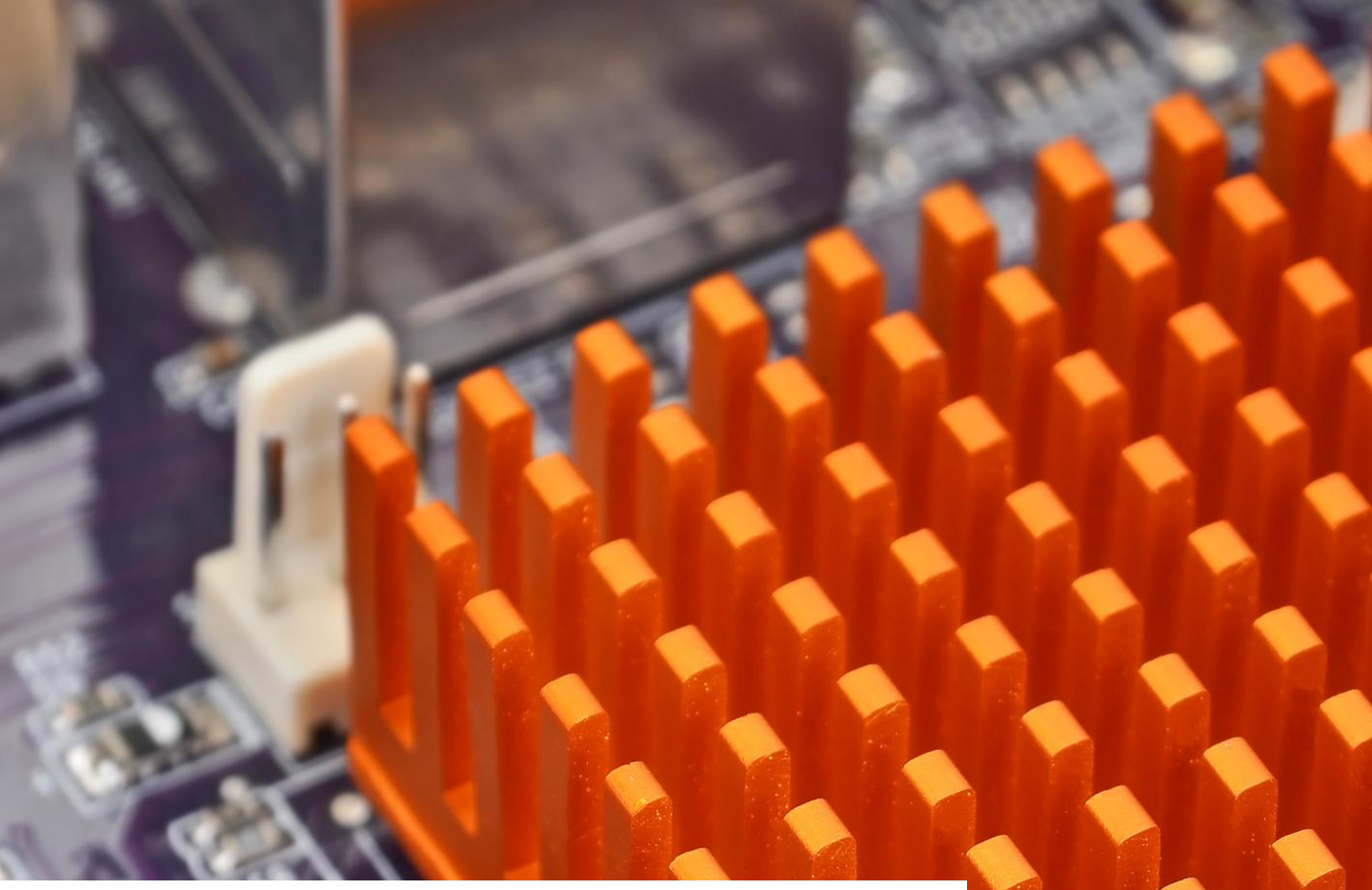


FPGA WEEK 2026

May 11-14, 2026

altera™

LATTICE SEMICONDUCTOR

MICROCHIP

📍 **Bologna**
ZanHotel Centergross
Bentivoglio,
Bologna

ARROW

FPGA WEEK 2026

Arrow is pleased to inform you that the dates for **FPGA Week 2026** have been confirmed.
The event will be held in **Bologna, Italy, from May 11 to May 14, 2026**.

The event will give you the opportunity to learn all news and updates from **Arrow FPGA suppliers: Altera, Lattice and Microchip**.
The event is dedicated to senior and beginner FPGA designers. During the workshop, participants will get an overview and perform exercises on FPGA evaluation boards provided by Arrow.

The **first day** of the event will be dedicated to **Timing Constraints and Static Timing Analysis**.
The **following three days** will be dedicated to **hands-on exercise sessions** delivered by the three vendors: **Altera, Microchip, and Lattice**.
These sessions will consist of **practical, hands-on exercises**, carried out on participants' own PCs using **development boards provided by Arrow**.

Sessions are repeated to allow everyone to participate avoiding having many people during hands-on. Anyone will have the opportunity to perform all sessions.

The event is limited in number.
You will receive the confirmation of your participation.

During the event, the showcase will host:
Advanced Energy, Altera, Cubit, DEDA Connect, Diodes, Enktron, Everspin, FAE Technology, GEB, Lattice, Lauterbach, NCAB Group, Microchip, Skyworks.

We look forward to welcoming you to FPGA Week 2026.

IN COLLABORATION WITH

May 11, 2026

DAY 1	ROOM 1	ROOM 2
14:00 – 14:30	**Welcome Coffee Registration**	
14:30 – 16:15	**STA introduction, Core Timing and Default STA**	
16:15 – 16:30	**Break**	
16:30 – 18:15	**Timing Exceptions and I/O Interfaces**	
From 19:15	**Supplier Dinner**	

Microchip – STA introduction, Core Timing and Default STA
This section provides a brief introduction to Static Timing Analysis (STA) and explains Libero SoC enhanced constraint flow. The training session will demonstrate utilize the graphical user interface (GUI) effectively to provide proper constraints and get access to relevant reports. We will explore the core timing constraints required for analysis. Once clocks are defined, we will discuss setup and hold analysis, with a specific focus on identifying the correct clock edges for default analysis. Additionally, we will address the handling of asynchronous signals and review recovery and removal analysis. Finally, we will see how Jitter can be properly considered.

Microchip – Timing Exceptions and I/O Interfaces
"Building on the default analysis covered in the first section, we will address timing exceptions, including their necessity and the rationale for specifying them. Key topics will include false paths, clock groups, multicycle exceptions, and minimum/maximum delay constraints. Finally, we will focus on I/O interfaces, discussing both synchronous and source-synchronous types. After a brief review of the principles underlying these interfaces, we will provide guidance on how to properly constrain them from a static timing analysis perspective."

May 12, 2026

DAY 2	ROOM 1	ROOM 2	ROOM 3
08:45 – 09:00	**Welcome Coffee Registration**		**Showcase**
09:00 – 10:45	**Microchip** – Implementing a basic Libero® SoC Project	**Altera -** Quartus Prime My First FPGA and Nios V LABs	
10:45 – 11:15	**Break**		
11:15 – 13:00	**Lattice –** Radiant Tutorial	**Microchip** – Implementing a basic Libero® SoC Project	
13:00 – 14:00	**Lunch**		
14:00 – 14:30		**AEI**	
14:30 – 15:00		**FAE Technology**	
15:00 – 15:15	**Break**		
15:15 – 17:00	**Altera –** Quartu Prime My First FPGA and NiosV Labs	**Lattice –** Radiant Tutorial (1)	
17:00 – 17:30		**CUBIT**	
17:30 – 18:00		Open	
From 20:30	**Supplier Dinner**		

Microchip – Implementig a basic Libero SoC Project
The first exercise presents the implementation of an example in which two FPGA boards are connected via Ethernet at Layer 1, without any MAC support. The exercise involves implementing the GMII interface starting from provided VHDL source code, going through all development phases up to implementation and debugging on an evaluation board. Particular attention is given to timing constraints to allow the FPGA to communicate with the Ethernet PHY at 125 MHz.

ALTERA – Quartus Prime PRO My First FPGA lab and NiosV Implementation lab
These 2 first labs from Altera are focused on new Agilex3 C devices family.
Those 2 exercises comes from a set of seven exercises specifically created to demonstrate Agielx3 utilization.
Following “Quartus Prime Pro my First FPGA” you’ll be able to understand how to use the Altera tool to setup from scratch a new project with an easy VHDL implementation.
In the lab named “NiosV Implementation” you’ll able to create/modify a SofCore NiosV HW structure and related SW to let understand how to use Agilex3 devices to integrate MPUs architectures

Lattice – Radiant Tutorial
This exercise focuses on using the tool from code development all the way to generating the programming file. Throughout the lab, the main design stages will be examined, with particular emphasis on timing constraints. You will learn how to apply constraints both before and after synthesis using the Constraint Editor, and how to analyze the results with the Timing Analyzer.

May 13, 2026

DAY 3	ROOM 1	ROOM 2	ROOM 3
08:45 – 09:00	**Welcome Coffee Registration**		**Showcase**
09:00 – 10:45	**Microchip** – HW–SW co-design example in Libero SoC	**Lattice –** Implementing a webcam in FPGA: MIPI to USB	
10:45 – 11:15	**Break**		
11:15 – 13:00	**Altera –** Timing Closure and SignalTap	**Microchip** – HW–SW co-design example in Libero SoC	
13:00 – 14:00	**Lunch**		
14:00 – 14:30		**NCAB Group / DVS**	
14:30 – 15:00		**GEB Enterprise**	
15:00 – 15:15	**Break**		
15:15 – 17:00	**Lattice –** Implementing a webcam in FPGA: MIPI to USB	**Altera –** Timing Closure and SignalTap	
17:00 – 17:30		**ENKTRON**	
17:30 – 18:00		Open	
From 20:30	**Supplier Dinner**		

Microchip – HW–SW co-design example in Libero SoC
This project aims to implement a hardware-based Ethernet packet filtering mechanism in VHDL on the SmartFusion2 FPGA to reduce the processing burden on the integrated Cortex-M3 software network stack. The system analyzes Ethernet frames in real time at MAC and IP levels, extracting source addresses and comparing them with configurable whitelist or blacklist tables. Packet acceptance or rejection is decided entirely in hardware, blocking unauthorized traffic before it reaches software. Configuration, statistics, and operating modes are managed by a Cortex-M3 application via dedicated registers, enabling efficient hardware–software separation.

ALTERA – Timing Closure and SignalTap
Following the "Timing Closure" lab the user will be able to front Timing closure "issues" and learn how to solve it using properly Altera TimeQuest tool and the .SDC synthax, during post-synthesys (timing problem setup) and post-layout (timing verification)
On the other lab named "SignalTap" user will follow an example to use this Altera tool useful to make functional HW verification (not Timing) using spare resources of the FPGA. SignalTap is de-facto a Digital Logic Analyzer able to sample path inside FPGA and proposing sample results on Debug PC via JTAG channel.

Lattice – Implementing a webcam in FPGA: MIPI to USB
This lab focuses on analyzing and completing the Lattice reference design that implements a MIPI-to-USB UVC bridge.
The first part of the exercise is dedicated to studying the SoC block based on RISC-V along with the custom peripherals responsible for routing the video stream to the USB interface.
In the second part, you will implement the video processing pipeline, which converts the RAW camera stream into YUV video in AXI-Stream format, applying algorithms such as debayering, color correction matrix, and others.

May 14, 2026

DAY 4	ROOM 1	ROOM 2
08:00 – 08:30	**Welcome Coffee Registration**	
08:30 – 10:00	**Lattice -** implementing a multiboot project	**Microchip** – Asymmetric SW implementation on PolarFire SoC
10:00 – 11:30	**Altera –** FPGA AI Suite and MiPi labs	**Lattice -** implementing a multiboot project
11:30 – 12:00	**Break**	
12:00 – 13:30	**Microchip** – Asymmetric SW implementation on PolarFire SoC	**Altera –** FPGA AI Suite and MiPi labs
13:30 – 14:30	**Lunch**	

Microchip – Asymmetric SW implementation on PolarFire SoC
This exercise showcases how a heterogeneous multicore SoC can combine high-level orchestration with real-time responsiveness, while achieving precise alignment across multiple platforms. A Linux cluster running on several cores manages system configuration and ethernet protocols, while a dedicated bare-metal core ensures immediate reaction to critical hardware events. Synchronization between boards leverages hardware timestamping at the MAC layer, fully compliant with IEEE 1588 Precision Time Protocol, enabling deterministic behavior and consistent execution across distributed nodes. This approach illustrates an architecture widely adopted in industrial environments where flexibility, cooperation, and repeatable timing are essential.

ALTERA – FPGA AI Suite and MiPi labs
During the "FPGA AI Suite" lab customer will have the opportunity to follow an introduction to AI and then implement in FPGA an AI model using OpenVino (model conversion and optimization) and Quarts tools (FPGA AI suite implementation and compilation).
In case there will be enough time also a MiPi CSI2 channel implementation is available; Mira220 Osram camera will be used with Agilex3 devboard to capture video from a MiPi channel.

Lattice – Implementing a multiboot project
In this lab, a practical usage example will be explored: managing multiboot mode. Four simple projects will be created and stored in separate sections of the SPI Flash memory.
In user mode, using the CONFIG_LMMIC primitive, the projects can be alternately loaded onto the FPGA through push-button interaction.
This allows the user to select one of the images stored in the SPI Flash and reconfigure the device with the desired image during operation.

Register now!

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